Analogue design and verification Engineer

Report to: Chief Technology Officer (CTO)

Locations: London UK

Salary: Competitive, depending on qualifications and experience

Job type: Full time, fixed contract with prospect for permanent position

Job description:

The Engineer - Analogue design and verification will join a small dynamic team that aims to develop a novel memory technology. The Engineer will be working closely with the engineering team and will undertake various engineering activities within the team where the individual will have the opportunity to make a significant impact.

A key aspect of the role is to design and develop the architecture for bespoke memory chips that will meet the rising technological demand, reflecting all aspects from specification development, sign-off to test chip design and foundry process evaluation. The successful candidate will have a strong memory chip and compiler design background (transistor level design and verification) with considerable industrial experience and will be able to demonstrate a thorough understanding of the issues related to IP delivery.

Key responsibilities:

- Write detailed analogue architecture specifications
- Work with silicon design, verification, and validation teams to guide successful product implementation
- Undertake transistor level design, simulation and layout using industry standard EDA tooling
- Develop the automated layout and verification flows in EDA tools
- Data and statistical analysis
- Design methodology development and optimisation
- Layout verification – Layout Versus Schematic (LVS) & Design Rule Check (DRC)
- Identify and submit patents of patentable circuit/architectural design features
- Select and integrate IP blocks, working with both internal design teams and external vendors

Job requirements:

- The candidate should possess a Bachelor or Master of Science degree in Computer Science, Electrical & Electronic Engineering, Material Science, or others, with 7+ years of directly relevant experience
- At least 5 years' experience of non-volatile memory chip design (FeRAM, MRAM, PCM, ReRAM, or Flash), embedded and/or standalone memory chips
- Experience in writing detailed architecture specifications for complex silicon devices
- Experience in physical synthesis and layout verification
- Experience of low power memory chip design in Advanced FinFET nodes

- Experience in C or C++ programming and other programming languages such as Perl or Python, and evidence of strong scripting skills
- Understanding of structure and issues of mainstream memory chips
- Experience of running commercial EDA tools and knowledge of potential issues
- Understanding of DFT, yield and design for manufacturability (DFM) issues
- Experience of taking designs into production
- Strong understanding of statistical analysis, strong analytical and problem-solving skills
- Ability to plan, coordinate and take responsibility for effective and on-time completion of project activities
- Self-motivated and creative with a passion for achieving success and excellence
- Strong interpersonal and communication skills with infectious enthusiasm and tenacity
- Excellent organizational and team working skills

Company:

The company is a semiconductor start-up developing emerging non-volatile memory (NVM) technologies with proprietary intellectual property. Headquartered in London, UK, they are a spin-off company from world leading institution Imperial College London. The company's ambition is to commercialise scientific innovation and they are looking to add experienced experts to join the team in London to develop their memory technology. Apply to become a part of a future leader in semiconductor chip technology and join a dynamic fast- paced working environment with an ambitious and success-focused team.

If you feel you are a suitable candidate and would like to work for this reputable company, then please do not hesitate in applying.